UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,503	10/25/2002	William R. Corbin	BUR920010217US1	2123

24241 7590 06/28/2005

IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
1000 RIVER STREET
972 E
ESSEX JUNCTION, VT 05452

EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,503	CORBIN ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *1-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/24/2005 has been entered.

Response to Amendment

2. This Office Action is in response to Amendment filed 4/27/2005, in reply to the Final Office Action dated 1/27/2005. Claims 1-14 are pending and presently under examination.

Objection to the drawings and specification for failing to show "isolation elements" is hereby withdrawn in view of corrected drawings submitted with replacement sheets for Figure 1 and 2. The drawings were received on 4/27/2005. These drawings are acceptable.

Objection of Claims 1-11 is hereby withdrawn in view of the Amendment.

Rejection of Claims 1-14 under 35 U.S.C. 112, first paragraph, is hereby withdrawn for the same reasons given for the withdrawal of the Objection to the drawings and specification, above.

Claim Rejections, for Claims 1-14 rejected under 35 U.S.C. 112, second paragraph, in reference to term " whereby", and for omitting essential structural cooperative relationships of elements, is hereby withdrawn in response to the corrections made by the Amendment.

Claim Objections

3. Claims 1-11 are objected to because of the following informalities:

Claim 1 includes limitations "of logic and memory" enclosed within parenthesis, and therefore such limitations do not carry patentable weigh. The use of the limitations enclosed within the parenthesis is to be considered as having no effect on the scope of the claims. Appropriate correction is required, by removing the limitations in the parenthesis or the parenthesis itself. See MPEP § 608.01(m). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the limitations in the following claims:

Claims 1 and 12 recite the limitation "the logic scan chain results" in last line of the claims.

Claim 2 recites the limitation "the logic tests" in the claim.

Claim 8 recites the limitation "bypass mode" in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishi et al. (U.S. Patent No: 5,987,635) in view of Bhawmik (U.S. Patent No: 5,680,543) and further in view of Clark (U.S. Patent No: 6,650,589).

Regarding independent Claim 1, Kishi substantially discloses a semiconductor integrated circuit device (60) apparatus capable of simultaneously performing self-test on memory circuits (20) and logic circuits (10) including a memory BIST circuit (71), Figure 6, comprising:

Scan chain bypass isolation elements (selectors 16 through 18) to enable and disable the BIST (71) through the test mode (TM) signal 32, for conducting a test of a memory core 22 in the memory circuit unit 20, while the logic scan chain results from (scan path 31) are read out into (scan path circuit 21).

Kishi does not explicitly disclose "a clocking system including clocking isolation elements for logic and memory circuits having individual separate isolated independent clocking paths to each logic and memory macro circuits". However, Bhawmik, in analogous art, discloses a clock generator circuit 21 for generating a set of clock signals (CK_1-CK_n) each at corresponding rated clock frequencies f_1-f_n, associated with the scan chains 12_1 -12_n, respectively, and a clock control circuit 22, corresponding to clocking isolation elements, including multiplexers for selecting the appropriate clock, BIST circuit 10 of Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a clock generator with a clock control circuit in the BIST circuit of Kishi, as taught by Bhawmik, for the purpose of allocating clock signals to logic and memory circuits, since both logic and memory circuits of Kishi deploy scan chains for shifting test data, so that each chain is clocked at its rated frequency. Also, operating a Built-In-Self-Test (BIST) circuit having multiple clock regimes permits each regime to be clocked at its rated operating speed, thus optimizing testing.

Furthermore, the modified device of Kishi and Bhawmik does not explicitly disclose, voltage isolation elements for logic and memory circuits. However, Clark, in analogous art, discloses voltage isolation elements, such as voltage regulator 90 that provides one operating voltage to microprocessor core 20 and a separate operating voltage to memory block 40, (Figure 2, Clark).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a voltage regulator as taught by Clark in the modified semiconductor integrated device of Kishi and Bhawmik, so as maintain isolation between the logic and memory operating voltage, since an integrated circuit having a microprocessor core and a memory block may operate at different voltages. Therefore, the voltage regulator generates two operating voltages, one for the microprocessor core to satisfy power and performance criteria, and the other operating voltage for the memory block to provide acceptable noise margins and maintain stability of the memory cells within the memory block (Abstract, Clark).

Regarding Claim 2, Kishi discloses wherein the bypass isolation elements (selectors 16 through 18) are initiated by a control signal (test mode, TM, 32).

6. Claims 3-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishi et al. (U.S. Patent No: 5,987,635) in view of Bhawmik (U.S. Patent No: 5,680,543) in view of Clark (U.S. Patent No: 6,650,589) and further in view of Nayak (U.S. Patent No: 6,430,718).

Regarding Claims 3-6, Kishi substantially discloses the claimed invention as applied to the claim above. The combined device of Kishi, Bhawmik and Clark fails to explicitly disclose the claimed limitations of "the control signal is provided by a primary input from control circuit, wherein the control signal is provided by a latch, wherein the control signal is applied to a latch and wherein the latch provides the control signal to a multiplexer in each memory macro".

However, Nayak (U.S. Patent No: 6,430,718), in analogous art, discloses a TAP controller 28 in an integrated circuit 14 for receiving a test mode signal (TMS) from an external control circuit, such as automated test equipment (ATE), which is in compliance with IEEE Std. 1149.1 JTAG standard for testing numerous integrated circuits.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide a test mode signal from an external (ATE) using a compliant IEEE Std. 1149.1 JTAG standard as taught by Nayak in the combined device of Kishi, Bhawmik and Clark, since Kishi already discloses an IEEE Std. 1149.1 JTAG standard interface for accessing (TDI, TDO, TMS, and TCK) signals from an ATE. A person skilled in the art would use conventional ATE to provide test control and data to an integrated circuit under test, since conventional testers which forward test vectors in parallel and receive test results in parallel would advantageously speed up the overall test process while maximizing the available vector memory applied to the integrated circuit via multiple tester pins. The desired parallel-delivered and parallel-received test mechanism should beneficially operate within the constraints of the JTAG compliant integrated circuit and JTAG printed circuit board architecture by only slightly modifying the boundary scan circuitry of that architecture, (see Background of the invention, Nayak).

Regarding Claim 7, Kishi discloses wherein the control signal (test mode, TM, 32) places the apparatus into bypass mode (TEST MODE) by selecting the output of the (BIST) 71, which loads logic test patterns into the (scan path circuit 21).

Regarding Claim 8, Kishi discloses wherein after the BIST is (TM) Normal the apparatus is taken out of bypass mode (Test Mode) the results are unloaded. Thus, the data written in the memory core in the data write step ST1 is read on the basis of a test output signal 39B of the memory circuit unit 20 through the test data bus TB, the test address bus TA and the test memory control signal TC. It is checked whether or not the read data accords with an expected value, and the memory test of the memory circuit unit 20 is thus completed.

Regarding Claims 9-11, Kishi substantially discloses the claimed invention as applied to claims above. The combined device of Kishi, Clark and Nayak fails to explicitly disclose a clocking system, which includes a memory test clock, which allows a logic test pattern to be loaded and unloaded independent of the memory clock, wherein a signal to the clocking system is applied by an external tester to a clock multiplier and control circuit, and wherein a signal to the clocking system is applied by an external tester to a clock generator located on the semiconductor device. However, Bhawmik, in analogous art, discloses a clock generator circuit 21 for generating a set of clock signals (CK_1-CK_n) each at corresponding rated clock frequencies f_1-f_n, associated with the scan chains 12_1 -12_n, respectively, and a clock control circuit 22, corresponding to clocking isolation elements, including multiplexers for selecting the appropriate clock, BIST circuit 10 of Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a clock generator with a clock control circuit as taught by Bhawmik in the modified BIST circuit of Kishi, Clark and Nayak for the

purpose of allocating clock signals to logic and memory circuits, since both logic and memory circuits of Kishi deploy scan chains for shifting test data, so that each chain is clocked at its rated frequency. Also, operating a Built-In-Self-Test (BIST) circuit having multiple clock regimes permits each regime to be clocked at its rated operating speed, . thus optimizing testing.

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishi et al. (U.S. Patent No: 5,987,635) in view of Clark (U.S. Patent No: 6,650,589).

Regarding independent Claim 12, Kishi substantially discloses a method using a semiconductor integrated circuit device (60) capable of simultaneously performing self-test on memory circuits (20) and logic circuits (10) including a memory BIST circuit (71), Figure 6, comprising:

Clocking the logic (10) and memory circuits (20) using clock signal 30, Figure 6.

Enabling and disabling the BIST (71) scan chain bypass isolation elements (selectors 16 through 18) through the test mode (TM) signal 32, for conducting a test of a memory core 22 in the memory circuit unit 20, while the logic scan chain results from (scan path 31) are read out into (scan path circuit 21).

Kishi does not explicitly disclose, separating the logic and memory circuits using isolation elements.. However, Clark, in analogous art, discloses voltage isolation elements, such as voltage regulator 90 that provides one operating voltage to

microprocessor core 20 and a separate operating voltage to memory block 40, (Figure 2, Clark).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a voltage regulator as taught by Clark in the semiconductor integrated device of Kishi, so as maintain isolation between the logic and memory operating voltage, since an integrated circuit having a microprocessor core and a memory block may operate at different voltages. Therefore, the voltage regulator generates two operating voltages, one for the microprocessor core to satisfy power and performance criteria, and the other operating voltage for the memory block to provide acceptable noise margins and maintain stability of the memory cells within the memory block (Abstract, Clark).

Regarding Claim 13, Kishi discloses testing the bypass isolation elements (selectors 16 through 18) by a control bypass signal (test mode, TM, 32).

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kishi et al. (U.S. Patent No: 5,987,635) in view of Bhawmik (U.S. Patent No: 5,680,543).

Regarding independent Claim 14, Kishi substantially discloses a method using a semiconductor integrated circuit device (60) capable of simultaneously performing self-test on memory circuits (20) and logic circuits (10) including a memory BIST circuit (71), Figure 6, comprising:

Verifying scan chain 31 and BIST (71) operation, Figure 6, as follows: In a scan test step ST2B, the test mode signal 32 is deactivated for the necessity of selecting a

normal path from the test bus group, and the scan test is carried out by using a scan path 31. Thus, the image processor 11, the memory control unit 13 and the selectors 16 through 18 are tested for their operations.

Loading BIST (71) patterns (internal data bus DIN) using global clocking (clock 30) during, a data write step ST1, Figure 2a. The test mode (TM) signal 32 is activated, so that the selectors (16-18) can select the test data bus TB, test address bus TA and test memory control signal TC, thereby inputting a write data to the memory circuit unit 20 through the internal data bus DIN.

Placing the device into a bypass mode wherein the memory macro circuits are isolated from the scan chains, by enabling and disabling the BIST (71) scan chain bypass isolation elements (selectors 16 through 18) through the test mode (TM) signal 32, for conducting a test of a memory core 22 in the memory circuit unit 20, while the logic scan chain results from (scan path 31) are read out into (scan path circuit 21).

Running the scan chains (31) in parallel with BIST (71), where, "the scan test can be carried out even during the data holding test by inhibiting the data read/write operation on the memory circuit unit 20 through deactivation of the chip select signal 35 by using the first chip select control signal 33C. Accordingly, the data holding test and the scan test, which are conventionally conducted independently of each other, can be carried out in parallel with each other, and hence, the time required for the test of the entire LSI can be shortened", as described in reference to Figure 6.

Kishi does not explicitly disclose, "generating separate test clock signals to both memory macro circuits and logic circuits". However, Bhawmik, in analogous art,

discloses a clock generator circuit 21 for generating a set of clock signals (CK_1-CK_n) each at corresponding rated clock frequencies f_1-f_n, associated with the scan chains 12_1 -12_n, respectively, and a clock control circuit 22, corresponding to clocking isolation elements, including multiplexers for selecting the appropriate clock, BIST circuit 10 of Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a clock generator with a clock control circuit in the BIST circuit of Kishi, as taught by Bhawmik, for the purpose of allocating clock signals to logic and memory circuits, since both logic and memory circuits of Kishi deploy scan chains for shifting test data, so that each chain is clocked at its rated frequency. Also, operating a Built-In-Self-Test (BIST) circuit having multiple clock regimes permits each regime to be clocked at its rated operating speed, thus optimizing testing.

Response to Arguments

9. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: 9/24/05

Randolph Building, 401 Dulany Street,
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

Date: 24 June 2005
Office Action: Non-Final Rejection